WHAT IS CLAIMED IS:

1. A display system comprising:

a light source for producing a beam of white light along a first light path;

a filter wheel on said first light path for filtering said beam of white light;

a motor connected to said filter wheel for spinning said filter wheel;

a motor control circuit electrically connected to said motor for receiving a digital speed control word and driving said motor;

a spatial light modulator on said first light path for receiving said filtered beam of light traveling along said first path and selectively modulating said filtered beam of light traveling along said first path to form an image; and

a controller for providing image data to said spatial light modulator and said digital speed control word to said motor control circuit, wherein said digital speed control word is dithered at least twice each revolution of said motor.

2. The display system of Claim 1, said motor control circuit providing commutation interrupts to said controller, wherein said controller writes a new digital speed control word to said motor control circuit each commutation interrupt.

3. The display system of Claim 1, said motor control circuit providing commutation interrupts to said controller, wherein said controller writes a new digital speed control word to said motor control circuit as often as each commutation interrupt.

4. The display system of Claim 1, said controller further comprising a hardware interrupt timer to generate interrupts, wherein said controller writes a new digital speed control word to said motor control circuit each interrupt.

5. The display system of Claim 1, said controller further comprising a hardware interrupt timer to generate interrupts, wherein said controller writes a new digital speed control word to said motor control circuit as often as each interrupt.

6. The display system of Claim 1, said controller calculating an n-bit desired motor speed word, a most significant m-bit portion of said desired motor speed word used as a base digital speed control word and the next most significant p bits used to determine a dither pattern for said digital speed control word.

7. The display system of Claim 6, said dither pattern incrementing said base digital speed control word for a number of interrupt periods determined by the binary value represented by said p bits.

8. The display system of Claim 6, said desired motor speed word having 16 bits, said digital speed control word having 8 bits, and said p bits comprising 2 bits used to determine which of four interrupt periods the digital speed control word will be incremented during.

9. A motor controller for controlling the speed of a motor, said motor control circuit comprised of:

a motor control circuit electrically connected to said motor for receiving a digital speed control word representing a desired motor speed and driving said motor;

a controller connected to said motor control circuit for providing said digital speed control word to said motor control circuit, said controller dithering said digital speed control word at least twice each revolution of said motor.

10. The motor controller of Claim 9, said motor control circuit providing commutation interrupts to said controller, wherein said controller writes a new digital speed control word to said motor control circuit each commutation interrupt.

11. The motor controller of Claim 9, said motor control circuit providing commutation interrupts to said controller, wherein said controller writes a new digital speed control word to said motor control circuit as often as each commutation interrupt.

12. The motor controller of Claim 9, said controller further comprising a hardware interrupt timer to generate interrupts, wherein said controller writes a new digital speed control word to said motor control circuit each interrupt.

13. The motor controller of Claim 9, said controller further comprising a hardware interrupt timer to generate interrupts, wherein said controller writes a new digital speed control word to said motor control circuit as often as each interrupt.

14. The motor controller of Claim 9, said controller calculating an n-bit desired motor speed word, a most significant m-bit portion of said desired motor speed word used as a base digital speed control word and the next most significant p bits used to determine a dither pattern for said digital speed control word.

15. The motor controller of Claim 14, said dither pattern incrementing said base digital speed control word for a number of interrupt periods determined by the binary value represented by said p bits.

16. The motor controller of Claim 14, said desired motor speed word having 16 bits, said digital speed control word having 8 bits, and said p bits comprising 2 bits used to determine which of four interrupt periods the digital speed control word will be incremented during.